

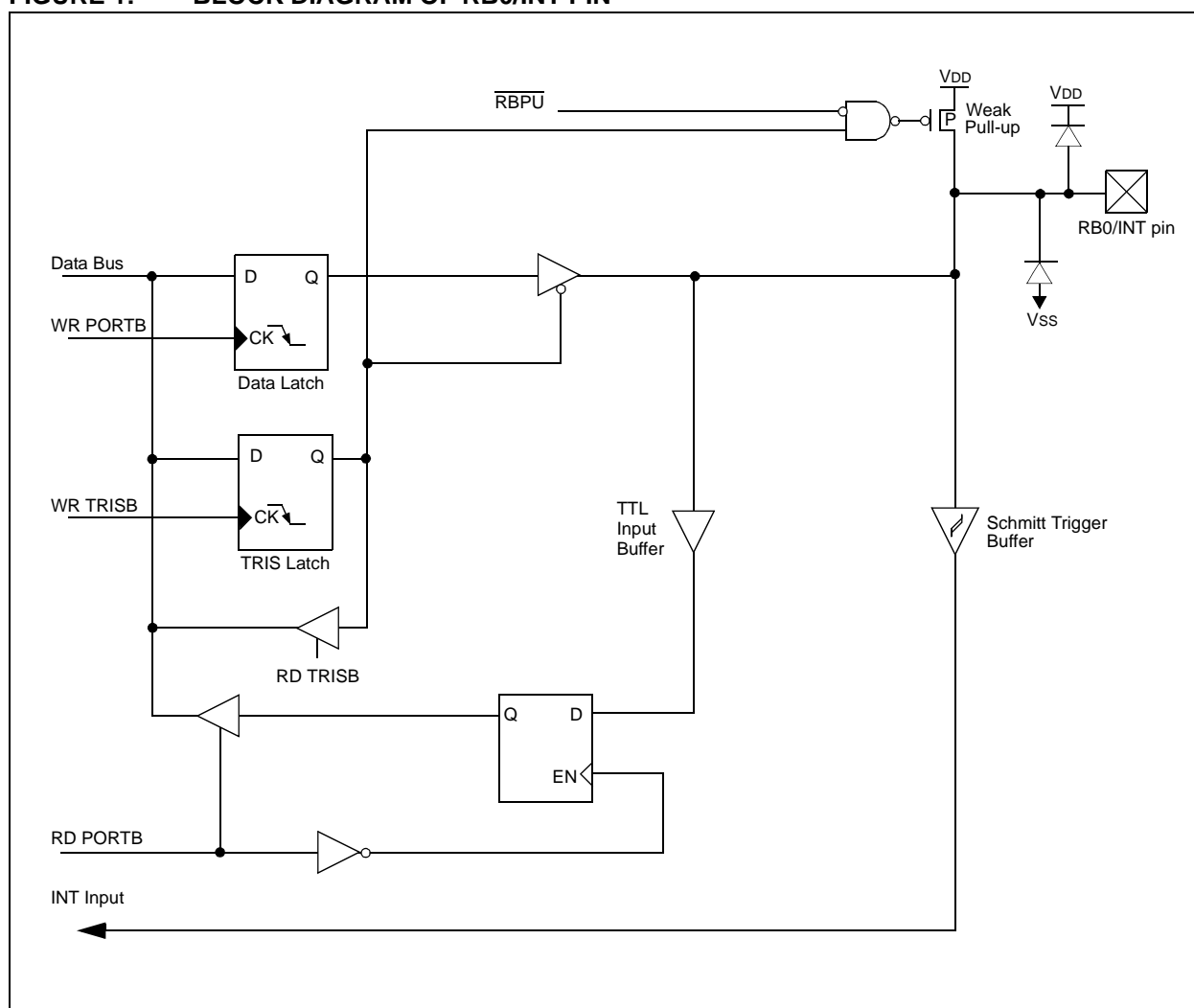
PIC16F62X Silicon/Data Sheet Errata

The PIC16F62X (Rev. A) parts you have received conform functionally to the Device Data Sheet (DS40300B), except for the anomalies described below.

1. Module: I/O Ports

A read of the PORTB Data Direction Register (TRISB) returns the Data Direction state on the port pins themselves and not the contents of the TRISB register latch.

FIGURE 1: BLOCK DIAGRAM OF RB0/INT PIN



PIC16F62X

FIGURE 2: BLOCK DIAGRAM OF RB1/TX/DT PIN

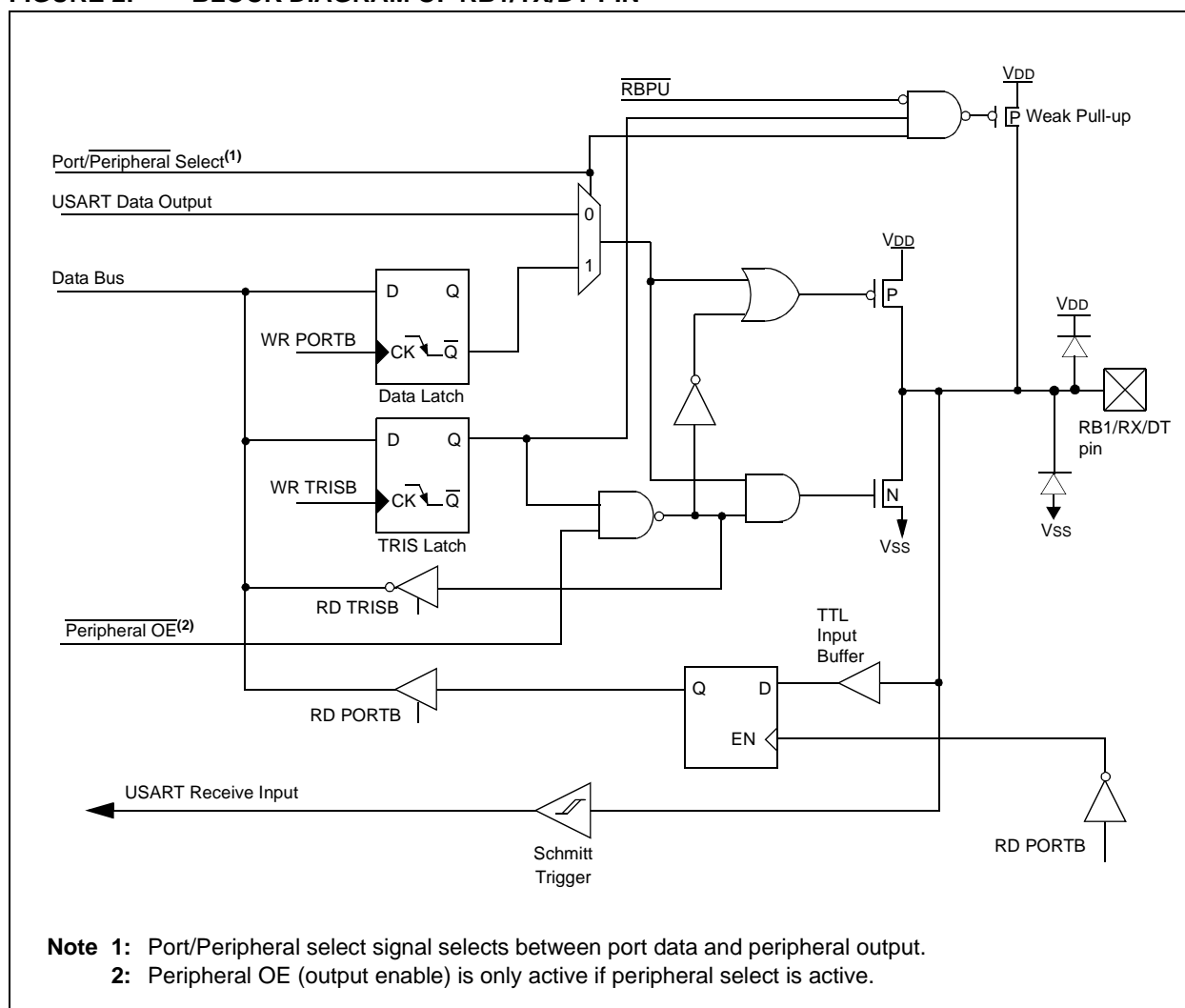
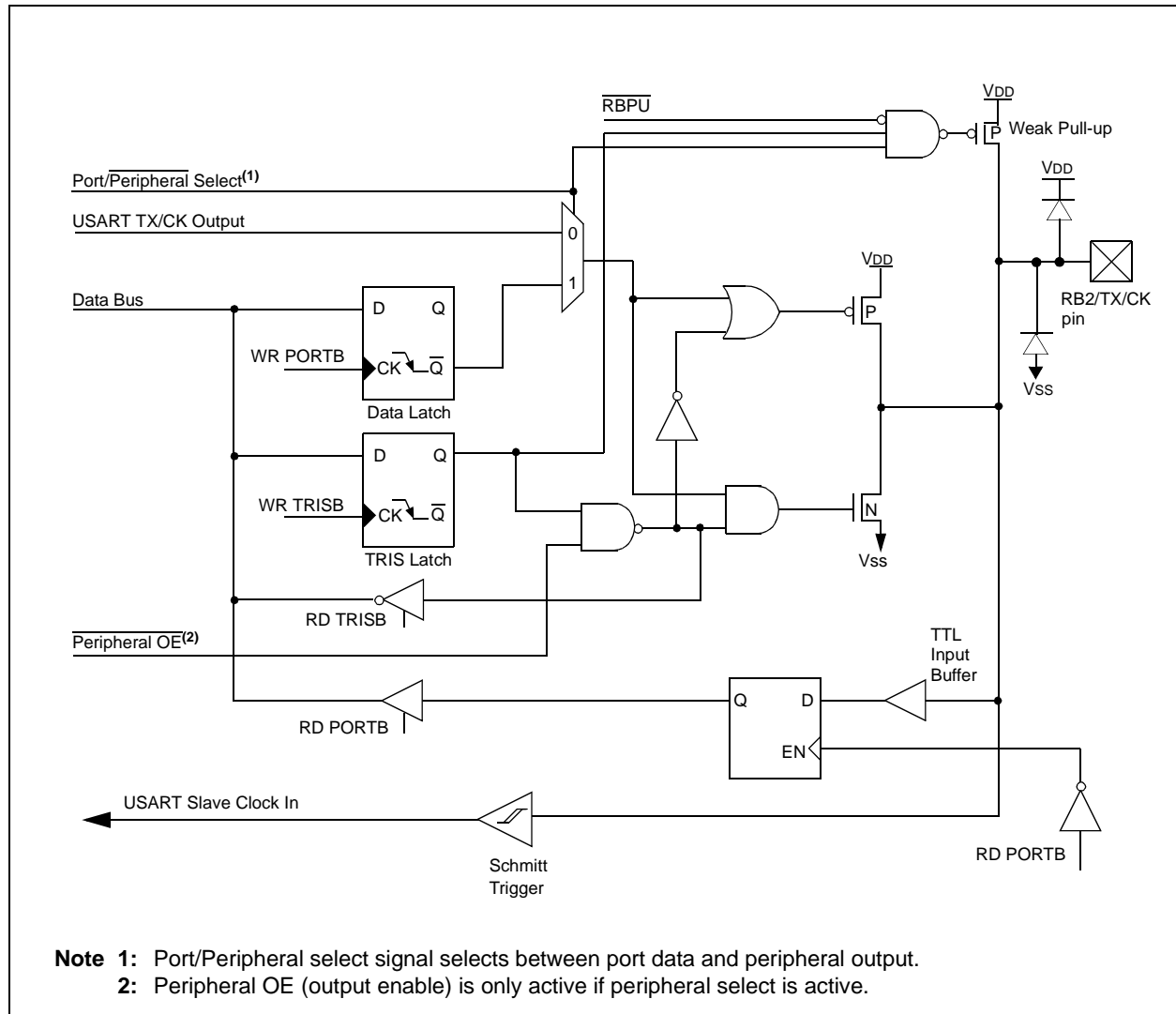


FIGURE 3: BLOCK DIAGRAM OF RB2/TX/CK PIN



PIC16F62X

FIGURE 4: BLOCK DIAGRAM OF THE RB3/CCP1 PIN

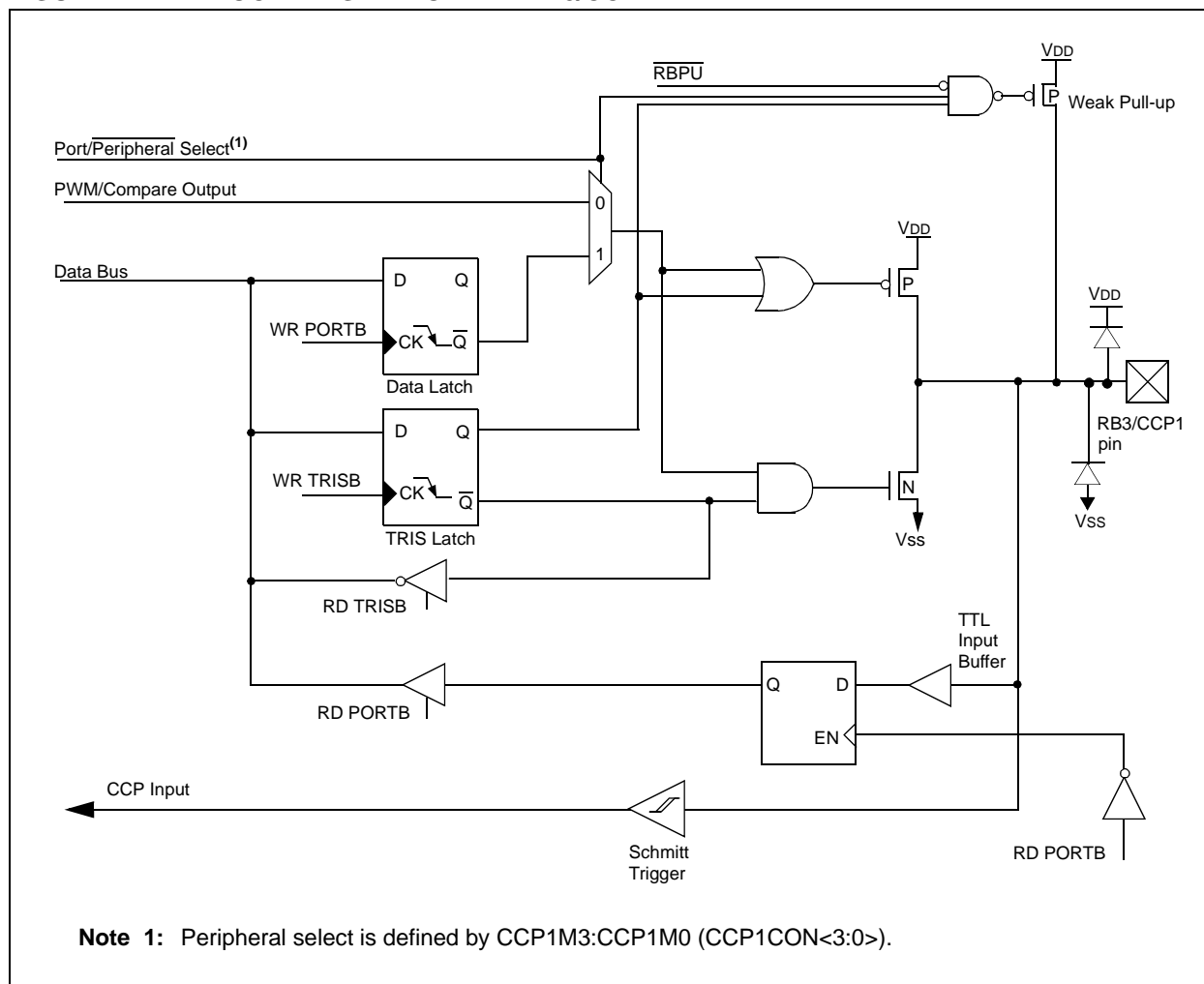
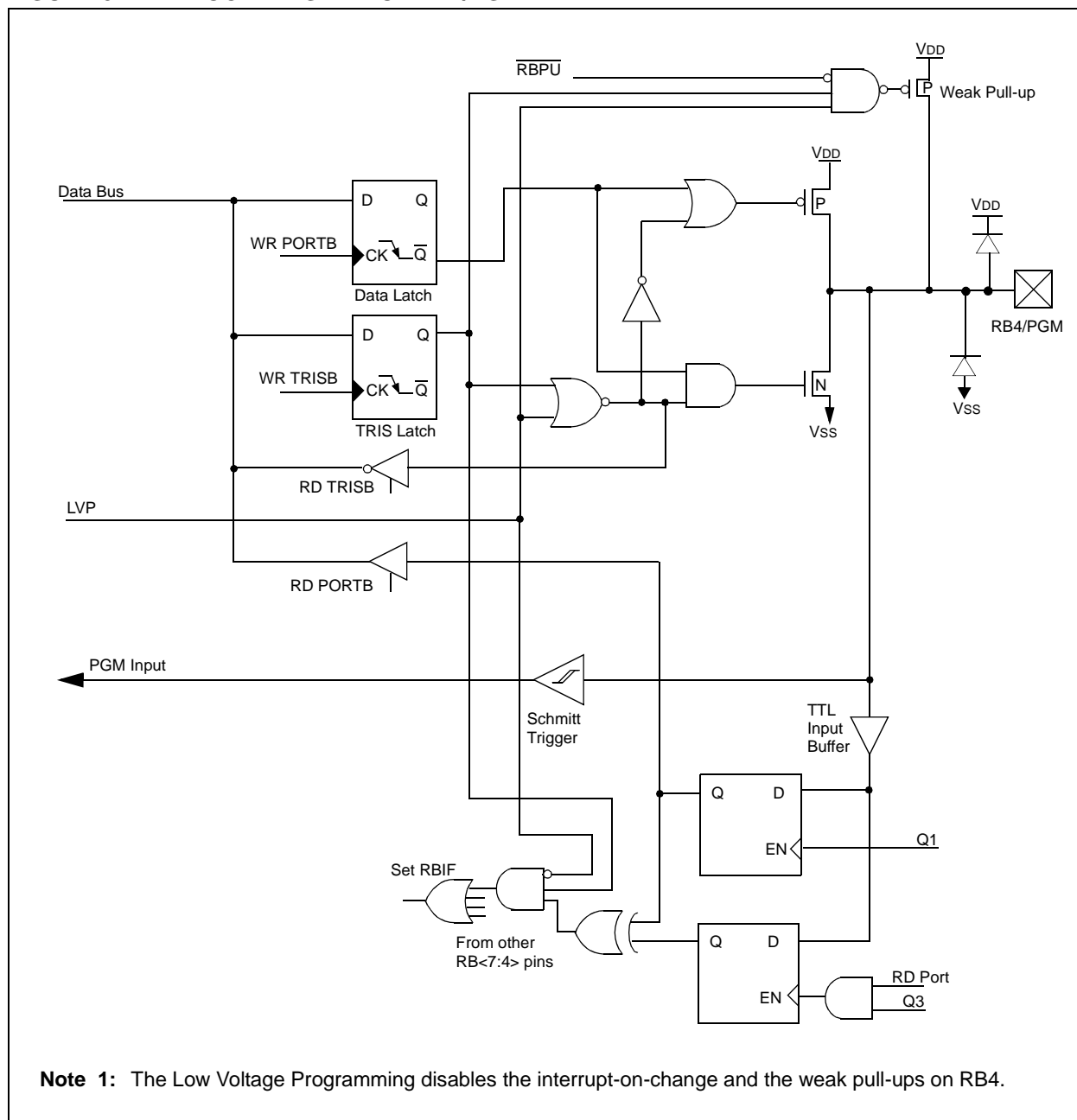


FIGURE 5: BLOCK DIAGRAM OF RB4/PGM PIN





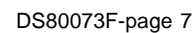
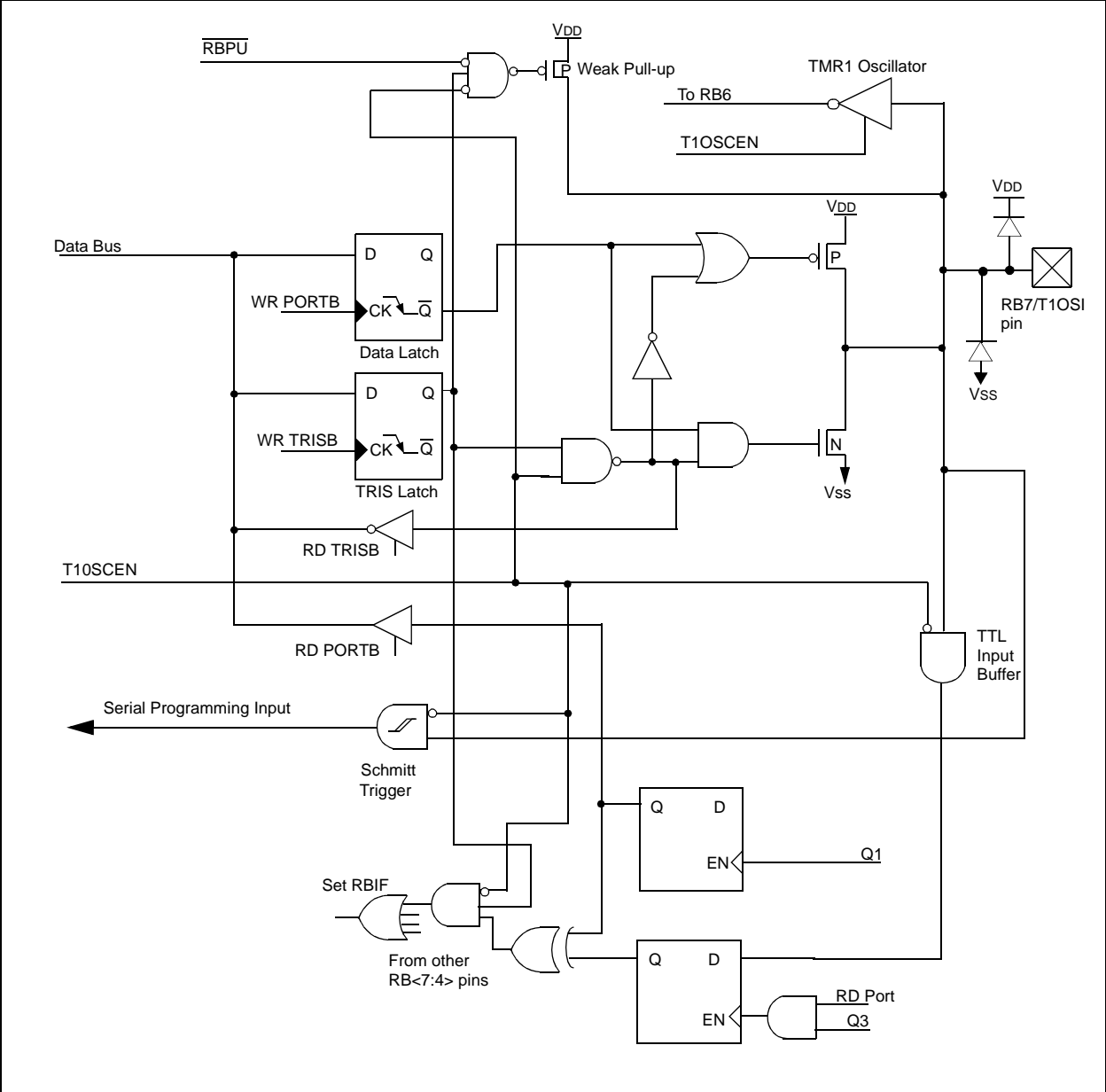


FIGURE 8: BLOCK DIAGRAM OF THE RB7/T10SI PIN



2. Module: Comparator Mode 1

Mode 1 allows AN2 to drive the (+) inputs of both comparators. AN1 continues to drive the (-) input of Comparator 2, but AN0 and AN3 can be switched into the (-) input of Comparator 1. The state of the CIS bit chooses which input is to be connected to the comparator. When CIS = 0, AN0 is attached and the comparator functions correctly. When CIS = 1, AN3 is not completely connected to the comparator, resulting in incorrect behavior.

Mode 2 is also a Multiplex mode using the CIS bit. This mode functions correctly.

All other modes are unaffected by this Errata.

3. Module: Low Voltage Programming Mode

The high voltage override for low voltage programming does not operate as specified in the programming specification. In the Low Voltage Programming (LVP) mode, the device can be programmed without using 12V on VPP (pin 4). However, when high voltage programming is used while the part has low voltage programming enabled, the Low Voltage mode is not overridden. If RB4 goes high for any reason during high voltage programming with LVP enabled, the programming will be interrupted.

Work around

Pull RB4 (pin 10) to ground during the initial programming to prevent programming interruptions. Once LVP has been disabled, it remedies this issue with RB4.

4. Module: CCP (Compare Mode)

The CCP1 output latch, observed on RB3/CCP1/P1A, can change unexpectedly when the CCP module is changed from a set output on match (CCP1CON<3:0> = "1000") to clear output on match (CCP1CON<3:0> = "1001") or vice versa. This condition will occur following a CCP Reset at the beginning of the third iteration of the following sequence.

- CCP1<3:0> is changed from "1001" to "1000" or vice versa.
- The TMR1H:TMR1L register pair matches the CCP1R1H:CCP1R1L register pair.

Step 1 of the third iteration will cause the CCP1 output latch to immediately and erroneously change to the inverse of the CCP1<0> bit. This gives the appearance of an inverted CCP response to the third and subsequent compare match events.

The apparent inverted response will persist until the CCP1CON<3> bit is cleared (exiting Compare mode). Interrupts always occur correctly on the match condition. The error is only in the state of the CCP1 output latch.

Work around

Option 1

Use the CCP toggle output on Compare Match mode (CCP1CON<3:0> = "0010").

Option 2

Since the problem occurs after two changes to the Compare and Match mode, it is only necessary to reset the CCP1CON register before the third change is made. To remain backwards compatible with earlier versions of the CCP module, always reset the CCP1CON register when changing from the clear output on Match mode to the set output on Match mode, as described in the following steps.

1. Ensure the RB3 data latch is set to 0.
2. Clear the CCP1CON register (`clrf CCP1CON`).
3. Set the CCP1CON<3:0> bits to "1000" for set output on match.

5. Module: MCLR/RA5 in LVP Mode

When the PIC16F62X device has LVP enabled, MCLR is always enabled, regardless of the CONFIG register settings.

PIC16F62X

Clarifications/Corrections to the Data Sheet:

In the Device Data Sheet (DS40300B), the following clarifications and corrections should be noted.

1. Module: T1SYNC (Register T1CON)

The bit T1SYNC in the Register T1CON (address 10h) should be asserted logic low (i.e., $\overline{\text{T1SYNC}}$). Table 4-1, page 15, and Table 10-2, page 65, of DS40300B should be listed as follows:

2. Module: ADEN (Register RCSTA)

The bit ADEN in Register RCSTA (address 18h), Table 4-1, is misspelled. The correct spelling should be ADDEN. This also appears in Figures and text on pages 72, 79, 80, 81, 82, 83, 84, 85, 86 and 89.

TABLE 4-1: SPECIAL REGISTERS SUMMARY BANK0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR Reset	Value on all other RESETS ⁽¹⁾
Bank 0											
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	--uu uuuu
18h	RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 -00x	0000 -00x

Legend: x = unknown, u = unchanged, - = unimplemented locations, read as '0', q = value depends on condition, shaded = unimplemented

Note 1: Other (non power-up) RESETS include $\overline{\text{MCLR}}$ Reset, Brown-out Detect and Watchdog Timer Reset during normal operation.

TABLE 10-2: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, AND TIMER1

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on all other RESETS
10h	T1CON	—	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	--00 0000	--uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by Capture and Timer1.

17.1 DC Characteristics: PIC16F62X-04 (Commercial, Industrial, Extended) PIC16F62X-20 (Commercial, Industrial, Extended)

DC Characteristics			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	VDD	Supply Voltage	3.0	—	5.5	V	
D002	VDR	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	VPOR	VDD start voltage to ensure Power-on Reset	—	VSS	—	V	See section on Power-on Reset for details
D004	SVDD	VDD rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details
D005	VBOD	Brown-out Detect Voltage	3.65 3.65	4.0 —	4.35 4.4	V V	BODEN configuration bit is set BODEN configuration bit is set, Extended
D010	IDD	Supply Current ⁽²⁾	—	—	0.7	mA	FOSC = 4.0 MHz, VDD = 3.0
			—	—	2.0	mA	FOSC = 4.0 MHz, VDD = 5.5*
D013			—	4.0	7.0	mA	FOSC = 20.0 MHz, VDD = 5.5
			—	—	6.0	mA	FOSC = 20.0 MHz, VDD = 4.5*
	D014		—	—	2.0	mA	FOSC = 10.0 MHz, VDD = 3.0*, Commercial
			—	—	10	μA	FOSC = 32 kHz, VDD = 3.0*
D020	IPD	Power-down Current ⁽³⁾	—	—	2.2	μA	VDD = 3.0, Commercial, Industrial
			—	—	5.0	μA	VDD = 4.5*, Commercial, Industrial
			—	—	9.0	μA	VDD = 5.5, Commercial, Industrial
			—	—	30.0	μA	VDD = 5.5, Extended
D022	ΔIWD	WDT Current ⁽⁴⁾	—	6.0	20	μA	VDD = 4.0V, Commercial, Industrial
					25	μA	VDD = 4.0V, Extended
D022A	ΔIBOD	Brown-out Detect Current ⁽⁴⁾	—	75	125	μA	BOD enabled, VDD = 5.0V
D023	ΔICOMP	Comparator Current for each Comparator ⁽⁴⁾	—	30	50	μA	VDD = 4.0V
D023A	ΔIVREF	VREF Current ⁽⁴⁾	—		135	μA	VDD = 4.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.

The test conditions for all IDD measurements in active Operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD, MCLR = VDD;
WDT disabled.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS.

4: The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base IDD or IPD measurement.

PIC16F62X

17.2 DC Characteristics: PIC16LF62X-04 (Commercial, Industrial)

DC Characteristics			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial				
			Operating voltage V_{DD} range as described in DC spec Table 17-1 and Table 12-2				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001	V_{DD}	Supply Voltage	2.0	—	5.5	V	
D002	V_{DR}	RAM Data Retention Voltage ⁽¹⁾	—	1.5*	—	V	Device in SLEEP mode
D003	V_{POR}	V_{DD} start voltage to ensure Power-on Reset	—	V_{SS}	—	V	See section on Power-on Reset for details
D004	SV_{DD}	V_{DD} rise rate to ensure Power-on Reset	0.05*	—	—	V/ms	See section on Power-on Reset for details
D005	V_{BOD}	Brown-out Detect Voltage	3.65	4.0	4.35	V	BODEN configuration bit is cleared
D010	I_{DD}	Supply Current ⁽²⁾	—	—	0.6	mA	FOSC = 4.0 MHz, V_{DD} = 2.0
			—	—	0.7	mA	FOSC = 4.0 MHz, V_{DD} = 5.5*
D013			—	4.0	7.0	mA	FOSC = 20.0 MHz, V_{DD} = 5.5
			—	—	6.0	mA	FOSC = 20.0 MHz, V_{DD} = 4.5*
D014			—	—	2.0	mA	FOSC = 10.0 MHz, V_{DD} = 3.0, Commercial
			—	—	TBD	μA	FOSC = 32 kHz, V_{DD} = 2.0*
D020	I_{PD}	Power-down Current ^{(2), (3)}	—	—	1.98	μA	V_{DD} = 2.0
			—	—	9.0	μA	V_{DD} = 5.5
D022	ΔI_{WDT}	WDT Current ⁽⁴⁾	—	6.0	15	μA	V_{DD} = 3.0V
D022A	ΔI_{BOD}	Brown-out Detect Current ⁽⁴⁾	—	75	125	μA	$\overline{\text{BOD}}$ enabled, V_{DD} = 5.0V
D023	ΔI_{COMP}	Comparator Current for each Comparator ⁽⁴⁾	—	30	50	μA	V_{DD} = 3.0V
D023A	ΔI_{VREF}	VREF Current ⁽⁴⁾	—	—	135	μA	V_{DD} = 3.0V

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** This is the limit to which V_{DD} can be lowered in SLEEP mode without losing RAM data.
- 2:** The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature also have an impact on the current consumption.
The test conditions for all I_{DD} measurements in active Operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to V_{DD} ,
MCLR = V_{DD} ; WDT enabled/disabled as specified.
- 3:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD} or V_{SS} .
- 4:** The Δ current is the additional current consumed when this peripheral is enabled. This current should be added to the base I_{DD} or I_{PD} measurement.

17.3 DC Characteristics: PIC16F62X (Commercial, Industrial, Extended) PIC16LF62X (Commercial, Industrial)

DC Characteristics			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial and $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ for commercial and $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended				
			Operating voltage V_{DD} range as described in DC spec Table 17-1 and Table 12-2				
Param. No.	Sym	Characteristic	Min	Typ†	Max	Unit	Conditions
D030	V_{IL}	Input Low Voltage I/O ports: with TTL buffer	V_{SS}	—	0.8 0.15 V_{DD}	V	$V_{DD} = 4.5\text{V to } 5.5\text{V}$ otherwise
D031		with Schmitt Trigger input	V_{SS}	—	0.2 V_{DD}	V	
D032		$\overline{\text{MCLR}}$, RA4/T0CKI, OSC1 (in ER mode)	V_{SS}	—	0.2 V_{DD}	V	
D033		OSC1 (in XT and HS) OSC1 (in LP)	V_{SS} V_{SS}	— —	0.3 V_{DD} 0.6 V_{DD} -1.0	V V	
D040	V_{IH}	Input High Voltage I/O ports: with TTL buffer	2.0V .25 $V_{DD} + 0.8\text{V}$	— —	V_{DD} V_{DD}	V	$V_{DD} = 4.5\text{V to } 5.5\text{V}$ otherwise
D041		with Schmitt Trigger input	0.8 V_{DD}	—	V_{DD}	V	
D042		$\overline{\text{MCLR}}$ RA4/T0CKI	0.8 V_{DD}	—	V_{DD}	V	
D043		OSC1 (EC mode) OSC1 (XT, HS and LP)	0.8 V_{DD} 0.7 V_{DD}	— —	V_{DD} V_{DD}	V V	
D070	IPURB	PORTB weak pull-up current	50	200	400	μA	$V_{DD} = 5.0\text{V}$, $V_{PIN} = V_{SS}$
D060	I_{IL}	Input Leakage Current^{(1), (2)} I/O ports (except PORTA)			± 1.0	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, pin at hi-impedance
D061		PORTA	—	—	± 0.5	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, pin at hi-impedance
D063		RA4/T0CKI	—	—	± 1.0	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$
		OSC1, $\overline{\text{MCLR}}$	—	—	± 5.0	μA	$V_{SS} \leq V_{PIN} \leq V_{DD}$, XT, HS and LP osc configuration
D080	V_{OL}	Output Low Voltage I/O ports	—	—	0.6	V	$I_{OL} = 8.5\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40° to $+85^{\circ}\text{C}$
			—	—	0.6	V	$I_{OL} = 7.0\text{ mA}$, $V_{DD} = 4.5\text{V}$, $+125^{\circ}\text{C}$
D083		OSC2/CLKOUT (ER only)	—	—	0.6	V	$I_{OL} = 1.6\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40° to $+85^{\circ}\text{C}$
			—	—	0.6	V	$I_{OL} = 1.2\text{ mA}$, $V_{DD} = 4.5\text{V}$, $+125^{\circ}\text{C}$
D090	V_{OH}	Output High Voltage⁽²⁾ I/O ports (except RA4)	$V_{DD} - 0.7$	—	—	V	$I_{OH} = -3.0\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40° to $+85^{\circ}\text{C}$
			$V_{DD} - 0.7$	—	—	V	$I_{OH} = -2.5\text{ mA}$, $V_{DD} = 4.5\text{V}$, $+125^{\circ}\text{C}$
D092		OSC2/CLKOUT (ER only)	$V_{DD} - 0.7$	—	—	V	$I_{OH} = -1.3\text{ mA}$, $V_{DD} = 4.5\text{V}$, -40° to $+85^{\circ}\text{C}$
			$V_{DD} - 0.7$	—	—	V	$I_{OH} = -1.0\text{ mA}$, $V_{DD} = 4.5\text{V}$, $+125^{\circ}\text{C}$
D150	V_{OD}	Open Drain High Voltage		—	8.5	V	RA4 pin PIC16F62X, PIC16LF62X
D100	COSC2	Capacitive Loading Specs on Output Pins OSC2 pin		—	15	pF	In XT, HS and LP modes when external clock used to drive OSC1
D101	CIO	All I/O pins/OSC2 (in ER mode)		—	50	pF	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

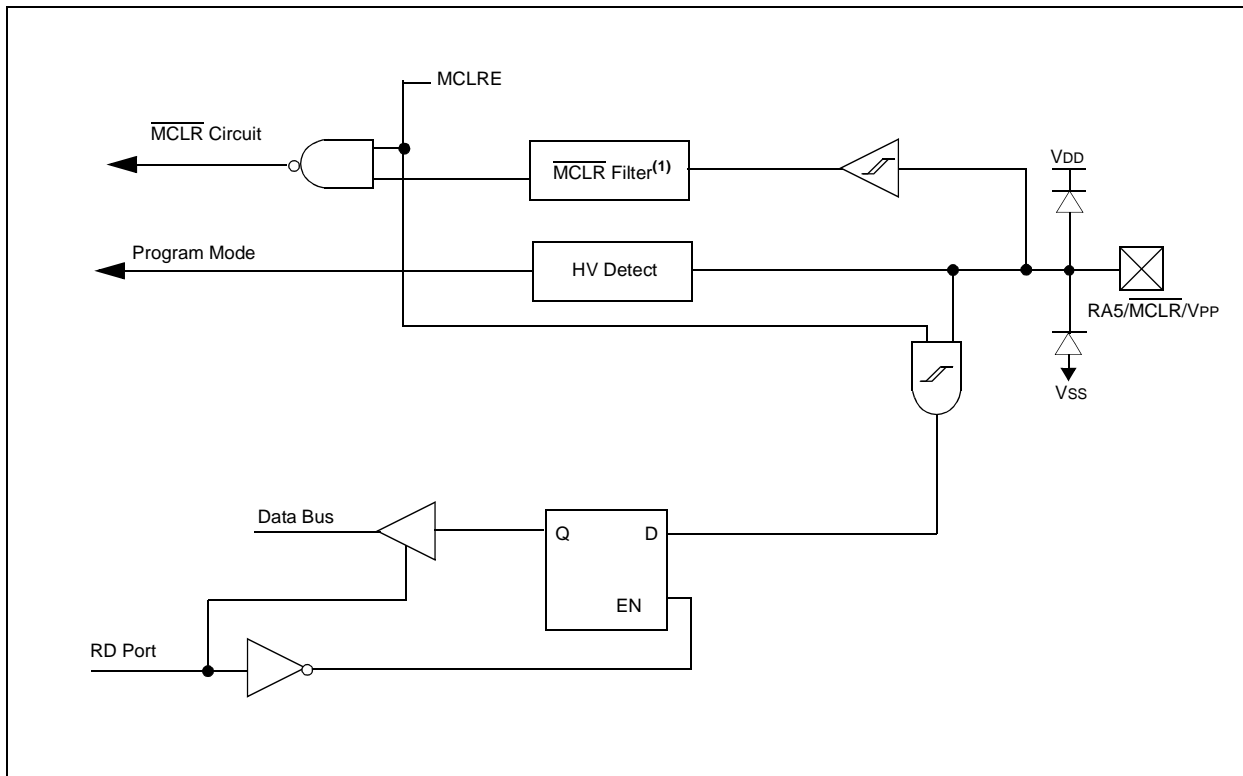
2: Negative current is defined as coming out of the pin.

PIC16F62X

3. Module: I/O Ports (RA5/MCLR/VPP)

The following block diagram shown in Section 5, Figure 5-5 is incorrect. The following figure should be used instead.

FIGURE 5-5: BLOCK DIAGRAM OF THE RA5/MCLR/VPP PIN



4. Module: Comparator

The example given in Section 9, Example 9-1, concerning “Initializing the Comparator Module” is incorrect. The following code example should be used instead.

EXAMPLE 9-1: INITIALIZING COMPARATOR MODULE

```
BCF          INTCON,GIE          ; Turn OFF Global Interrupts
BCF          INTCON,PEIE         ; Turn OFF Peripheral Interrupts
CLRF        PORTA               ; Init Port A
MOVLW       0X03                ; Init comparator mode
MOVWF       CMCON               ; CM<2:0> = 011
BSF         STATUS,RP0          ; Select BANK 1
MOVLW       0x07                ; Initialize Port A Direction
MOVWF       TRISA               ; Set RA<2:0> as Inputs
                                   ; RA<4:3> as outputs
                                   ; TRIS<5> always reads '0'

BCF         STATUS,RP0          ; Select BANK 0
CALL        DELAY10             ; Wait 10us for comparator output to become valid
                                   ; See Table 17-1 Parameter 301
MOVWF       CMCON,F             ; Read CMCON to end change condition
BCF         PIR1,CMIF           ; Clear pending interrupts
BSF         STATUS,RP0          ; Select BANK 1
BSF         PIE1,CMIE           ; Enable Comparator Interrupts
BCF         STATUS,RP0          ; Select BANK 0
BSF         INTCON,PEIE         ; Enable Peripheral Interrupts
BSF         INTCON,GIE          ; Global Interrupt Enable

; Insert Your code....

; Helper function is the Delay for 10us routine show below.

DELAY10      ; burns 8 cycles + the call for 10 cycles or 10us at 4Mhz
    goto $+1 ; goto the next instruction and burn 2 cycles
    call retlbl ; goto the next instruction and burn 2 more cycles
retlbl return ; go back and burn 2 cycles (actually done 2x for 4 cycles consumed)
```

PIC16F62X

5. Module: Data EEPROM

The examples given in Section 13, concerning the Data EEPROM are incorrect. The EEPROM registers are all located in Bank 1. The examples show the registers in Bank 0 and Bank 1. The following code examples should be used instead to use this feature.

EXAMPLE 13-1: DATA EEPROM READ

```
BSF    STATUS, RP0    ; Bank 1
MOVLW  CONFIG_ADDR    ;
MOVWF  EEADR           ; Address to read
BSF    EECON1, RD      ; EE Read
MOVF   EEDATA, W       ; W = EEDATA
BCF    STATUS, RP0     ; Bank 0
```

EXAMPLE 13-2: DATA EEPROM WRITE

```
; set up the data and the address
BSF    STATUS, RP0    ; Bank 1
MOVLW  CONFIG_ADDR    ;
MOVWF  EEADR           ; Address to write
MOVLW  CONFIG_DATA     ;
MOVWF  EEDATA          ; Data to write

; perform the write operation
BSF    EECON1, WREN    ; Enable Write
BCF    INTCON, GIE     ; Disable INTs
MOVLW  055h            ;
MOVWF  EECON2           ; Write 55
MOVLW  0AAh            ;
MOVWF  EECON2           ; Write AA
BSF    EECON1, WR       ; Set WR bit
BCF    STATUS, RP0     ; Bank 0
```

EXAMPLE 13-3: DATA EEPROM VERIFY

```
; after the write is complete (i.e. in the
; write interrupt)
BSF    STATUS, RP0    ; Bank 1
MOVF   EEDATA, W       ; load the last
                        ; written value into W
BSF    EECON1, RD      ; start a read
;
; Is the value written (in W Reg) and
; read (in EEDATA) the same?
;
SUBWF  EEDATA, W       ; the EEDATA has fresh
                        ; data
BTFSS  STATUS, Z       ; Is the Zero flag set?
GOTO   WRITE_ERR       ; NO, Write Error
                        ; YES, Good Write
                        ; continue program
```

6. Module: Comparator

Under Section 9.5 Comparator Outputs, in the fourth sentence, "When the CM<2:0> = 110 or 001, multiplexors...", remove "or 001".

REVISION HISTORY

Rev A Document (6/00)

Original errata document.

Rev B Document (11/00)

Issue 3 (CCP Compare Mode), Table 1 and 2 were added (page 2).

Under the Clarifications/Corrections Section, Item 1, Table 15-12 was updated with additional information (page 3).

Under the Clarifications/Corrections Section, the following Items were added:

Rev C Document (6/01)

Issues 2 and 3 were added.

Under Clarifications/Corrections, Items 2 and 3 were changed and Item numbers were renumbered accordingly.

Rev D Document (9/01)

Item 3 was rewritten (page 9).

Under the Clarifications/Corrections to the Data Sheet Section, the following items were changed:

Item 2, Tables 17.1 and 17.2, were updated with minor changes (page 11 and page 12).

Item 6 was added (page 16).

Rev E Document (2/02)

Item 4 was added, MCLR/RA5 in LVP mode (page 9).

Rev F Document (4/02)

Under Clarifications/Corrections, Item 2, Tables 17-1, 17.2 and 17.3 were updated with minor changes (pages 11, 12 and 13).

PIC16F62X

NOTES:

Note the following details of the code protection feature on PICmicro® MCUs.

- The PICmicro family meets the specifications contained in the Microchip Data Sheet.
- Microchip believes that its family of PICmicro microcontrollers is one of the most secure products of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the PICmicro microcontroller in a manner outside the operating specifications contained in the data sheet. The person doing so may be engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as “unbreakable”.
- Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our product.

If you have any further questions about this matter, please contact the local sales office nearest to you.

Information contained in this publication regarding device applications and the like is intended through suggestion only and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. No representation or warranty is given and no liability is assumed by Microchip Technology Incorporated with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Use of Microchip's products as critical components in life support systems is not authorized except with express written approval by Microchip. No licenses are conveyed, implicitly or otherwise, under any intellectual property rights.

Trademarks


The Microchip name and logo, the Microchip logo, FilterLab, KEELOQ, microID, MPLAB, PIC, PICmicro, PICMASTER, PICSTART, PRO MATE, SEEVAL and The Embedded Control Solutions Company are registered trademarks of Microchip Technology Incorporated in the U.S.A. and other countries.

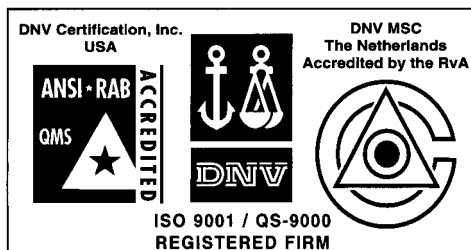
dsPIC, ECONOMONITOR, FanSense, FlexROM, fuzzyLAB, In-Circuit Serial Programming, ICSP, ICEPIC, microPort, Migratable Memory, MPASM, MPLIB, MPLINK, MPSIM, MXDEV, MXLAB, PICC, PICDEM, PICDEM.net, rfPIC, Select Mode and Total Endurance are trademarks of Microchip Technology Incorporated in the U.S.A.

Serialized Quick Turn Programming (SQTP) is a service mark of Microchip Technology Incorporated in the U.S.A.

All other trademarks mentioned herein are property of their respective companies.

© 2002, Microchip Technology Incorporated, Printed in the U.S.A., All Rights Reserved.

 Printed on recycled paper.



Microchip received QS-9000 quality system certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona in July 1999. The Company's quality system processes and procedures are QS-9000 compliant for its PICmicro® 8-bit MCUs, KEELOQ® code hopping devices, Serial EEPROMs and microperipheral products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001 certified.



WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200 Fax: 480-792-7277
Technical Support: 480-792-7627
Web Address: <http://www.microchip.com>

Rocky Mountain

2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7966 Fax: 480-792-7456

Atlanta

500 Sugar Mill Road, Suite 200B
Atlanta, GA 30350
Tel: 770-640-0034 Fax: 770-640-0307

Boston

2 Lan Drive, Suite 120
Westford, MA 01886
Tel: 978-692-3848 Fax: 978-692-3821

Chicago

333 Pierce Road, Suite 180
Itasca, IL 60143
Tel: 630-285-0071 Fax: 630-285-0075

Dallas

4570 Westgrove Drive, Suite 160
Addison, TX 75001
Tel: 972-818-7423 Fax: 972-818-2924

Detroit

Tri-Atria Office Building
32255 Northwestern Highway, Suite 190
Farmington Hills, MI 48334
Tel: 248-538-2250 Fax: 248-538-2260

Kokomo

2767 S. Albright Road
Kokomo, Indiana 46902
Tel: 765-864-8360 Fax: 765-864-8387

Los Angeles

18201 Von Karman, Suite 1090
Irvine, CA 92612
Tel: 949-263-1888 Fax: 949-263-1338

New York

150 Motor Parkway, Suite 202
Hauppauge, NY 11788
Tel: 631-273-5305 Fax: 631-273-5335

San Jose

Microchip Technology Inc.
2107 North First Street, Suite 590
San Jose, CA 95131
Tel: 408-436-7950 Fax: 408-436-7955

Toronto

6285 Northam Drive, Suite 108
Mississauga, Ontario L4V 1X5, Canada
Tel: 905-673-0699 Fax: 905-673-6509

ASIA/PACIFIC

Australia

Microchip Technology Australia Pty Ltd
Suite 22, 41 Rawson Street
Epping 2121, NSW
Australia
Tel: 61-2-9868-6733 Fax: 61-2-9868-6755

China - Beijing

Microchip Technology Consulting (Shanghai)
Co., Ltd., Beijing Liaison Office
Unit 915
Bei Hai Wan Tai Bldg.
No. 6 Chaoyangmen Beidajie
Beijing, 100027, No. China
Tel: 86-10-85282100 Fax: 86-10-85282104

China - Chengdu

Microchip Technology Consulting (Shanghai)
Co., Ltd., Chengdu Liaison Office
Rm. 2401, 24th Floor,
Ming Xing Financial Tower
No. 88 TIDU Street
Chengdu 610016, China
Tel: 86-28-86766200 Fax: 86-28-86766599

China - Fuzhou

Microchip Technology Consulting (Shanghai)
Co., Ltd., Fuzhou Liaison Office
Unit 28F, World Trade Plaza
No. 71 Wusi Road
Fuzhou 350001, China
Tel: 86-591-7503506 Fax: 86-591-7503521

China - Shanghai

Microchip Technology Consulting (Shanghai)
Co., Ltd.
Room 701, Bldg. B
Far East International Plaza
No. 317 Xian Xia Road
Shanghai, 200051
Tel: 86-21-6275-5700 Fax: 86-21-6275-5060

China - Shenzhen

Microchip Technology Consulting (Shanghai)
Co., Ltd., Shenzhen Liaison Office
Rm. 1315, 13/F, Shenzhen Kerry Centre,
Renminnan Lu
Shenzhen 518001, China
Tel: 86-755-2350361 Fax: 86-755-2366086

China - Hong Kong SAR

Microchip Technology Hongkong Ltd.
Unit 901-6, Tower 2, Metroplaza
223 Hing Fong Road
Kwai Fong, N.T., Hong Kong
Tel: 852-2401-1200 Fax: 852-2401-3431

India

Microchip Technology Inc.
India Liaison Office
Divyasree Chambers
1 Floor, Wing A (A3/A4)
No. 11, O'Shaugnessey Road
Bangalore, 560 025, India
Tel: 91-80-2290061 Fax: 91-80-2290062

Japan

Microchip Technology Japan K.K.
Benex S-1 6F
3-18-20, Shinyokohama
Kohoku-Ku, Yokohama-shi
Kanagawa, 222-0033, Japan
Tel: 81-45-471-6166 Fax: 81-45-471-6122

Korea

Microchip Technology Korea
168-1, Youngbo Bldg. 3 Floor
Samsung-Dong, Kangnam-Ku
Seoul, Korea 135-882
Tel: 82-2-554-7200 Fax: 82-2-558-5934

Singapore

Microchip Technology Singapore Pte Ltd.
200 Middle Road
#07-02 Prime Centre
Singapore, 188980
Tel: 65-6334-8870 Fax: 65-6334-8850

Taiwan

Microchip Technology Taiwan
11F-3, No. 207
Tung Hua North Road
Taipei, 105, Taiwan
Tel: 886-2-2717-7175 Fax: 886-2-2545-0139

EUROPE

Denmark

Microchip Technology Nordic ApS
Regus Business Centre
Lautrup høj 1-3
Ballerup DK-2750 Denmark
Tel: 45 4420 9895 Fax: 45 4420 9910

France

Microchip Technology SARL
Parc d'Activite du Moulin de Massy
43 Rue du Saule Trapu
Batiment A - 1er Etage
91300 Massy, France
Tel: 33-1-69-53-63-20 Fax: 33-1-69-30-90-79

Germany

Microchip Technology GmbH
Gustav-Heinemann Ring 125
D-81739 Munich, Germany
Tel: 49-89-627-144 0 Fax: 49-89-627-144-44

Italy

Microchip Technology SRL
Centro Direzionale Colleoni
Palazzo Taurus 1 V. Le Colleoni 1
20041 Agrate Brianza
Milan, Italy
Tel: 39-039-65791-1 Fax: 39-039-6899883

United Kingdom

Microchip Ltd.
505 Eskdale Road
Winnersh Triangle
Wokingham
Berkshire, England RG41 5TU
Tel: 44 118 921 5869 Fax: 44-118 921-5820

05/01/02